IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hisashi Ohtani	Art Unit	: Unknown
Serial No.	: New Divisional Application	Examiner	: Unknown
Filed	: September 9, 2003		
Title	: SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION METHOD THEREOF		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as indicated on the following pages.

Amendments to the Specification begin at page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.